DO NOT ENTER TM 12/21/04

Amendments to the Claims

1. (Currently Amended) Digital signal processing apparatus comprising a plurality of available hardware resource means and a first instruction set means having access to said available hardware resource means, so that at least a part of said hardware resource means execute operations under control of said first instruction set means;
the digital signal processing apparatus further comprising ~~characterized by~~ a second instruction set means having access to only a predetermined limited subset of said plurality of available hardware resource means, so that at least a part of said predetermined limited subset of said hardware resource means execute operations under control of said second instruction set means, wherein in case of an interrupt the state of all of said limited subset of hardware resource means are stored within a single clock cycle using a plurality of flip-flops and all hardware resource means under control of said first instruction set means have their state frozen.

2. (Original) Apparatus according to claim 1, wherein said available hardware resource means are processor resource means.